*Fig. 1*

	3 1	1 6	1 5	8 7	0
EAX		AH (100+!P)	AL (000)		
ECX		CH (101+!P)	CL (001)		
EDX		DH (110+!P)	DL (010)		
EBX		BH (111+!P)	BL (011)		
ESP			SPL (100+P)		
EBP			BPL (101+P)		
ESI			SIL (110+P)		
			DIL (111+P)		

Note: "+P" = Instruction Includes Register Address Prefix Byte
 "+!P" = Instruction Excludes Register Address Prefix Byte

Fig. 2

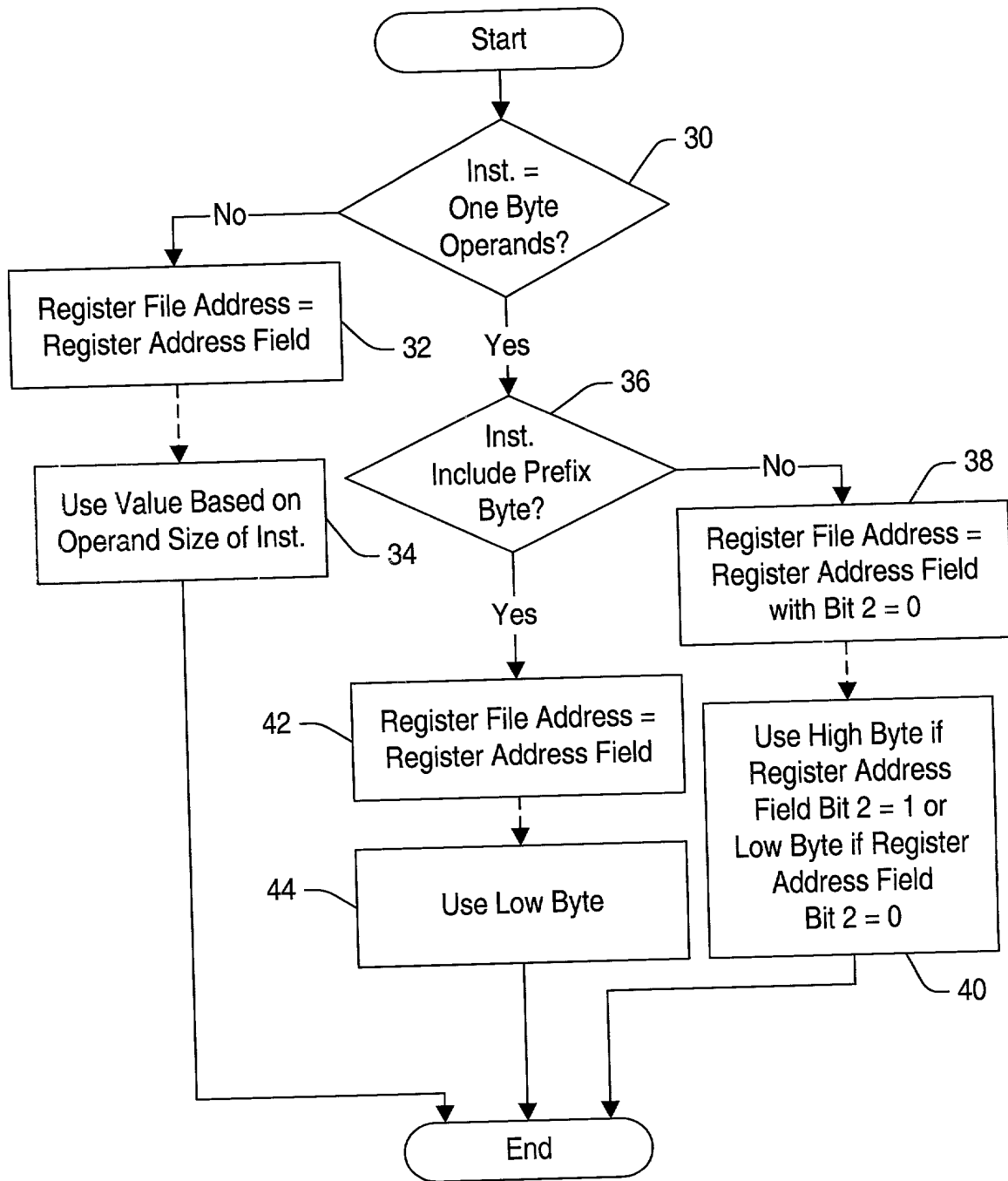


Fig. 3

	31 or 63	1 1 6 5	8 7	0
EAX		AH (x100+!P)	AL (0000+P or x000+!P)	
ECX		CH (x101+!P)	CL (0001+P or x001+!P)	
EDX		DH (x110+!P)	DL (0010+P or x010+!P)	
EBX		BH (x111+!P)	BL (0011+P or x011+!P)	
ESP			SPL (0100+P)	
EBP			BPL (0101+P)	
ESI			SIL (0110+P)	
EDI			DIL (0111+P)	
R8			R8B (1000+P)	
R9			R9B (1001+P)	
R10			R10B (1010+P)	
R11			R11B (1011+P)	
R12			R12B (1100+P)	
R13			R13B (1101+P)	
R14			R14B (1110+P)	
R15			R15B (1111+P)	

Note: "+P" = Instruction Includes Register Address Prefix Byte
"+!P" = Instruction Excludes Register Address Prefix Byte

Fig. 4

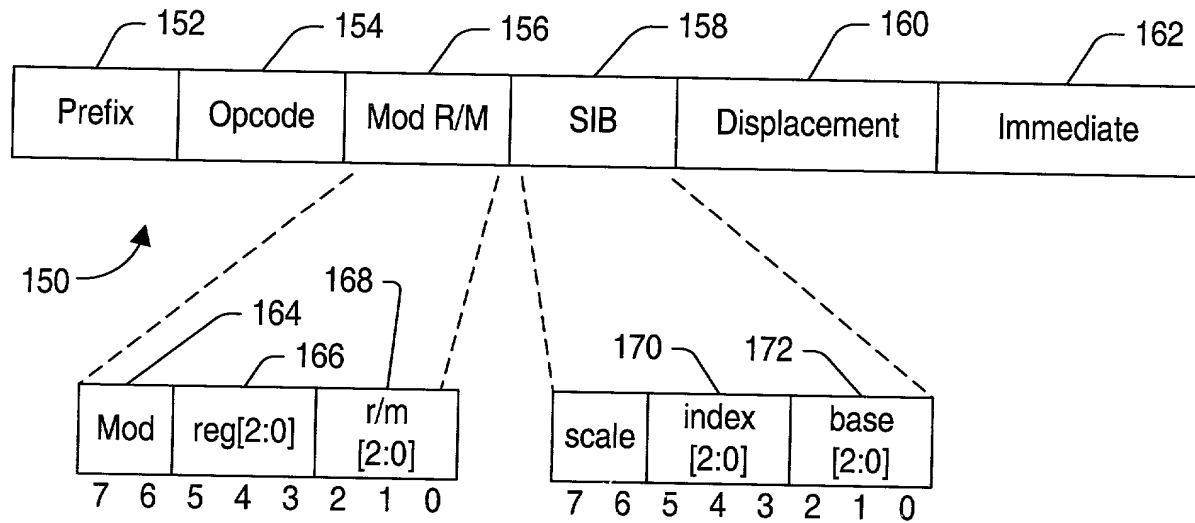


Fig. 5

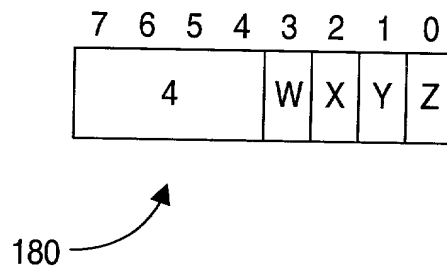


Fig. 6

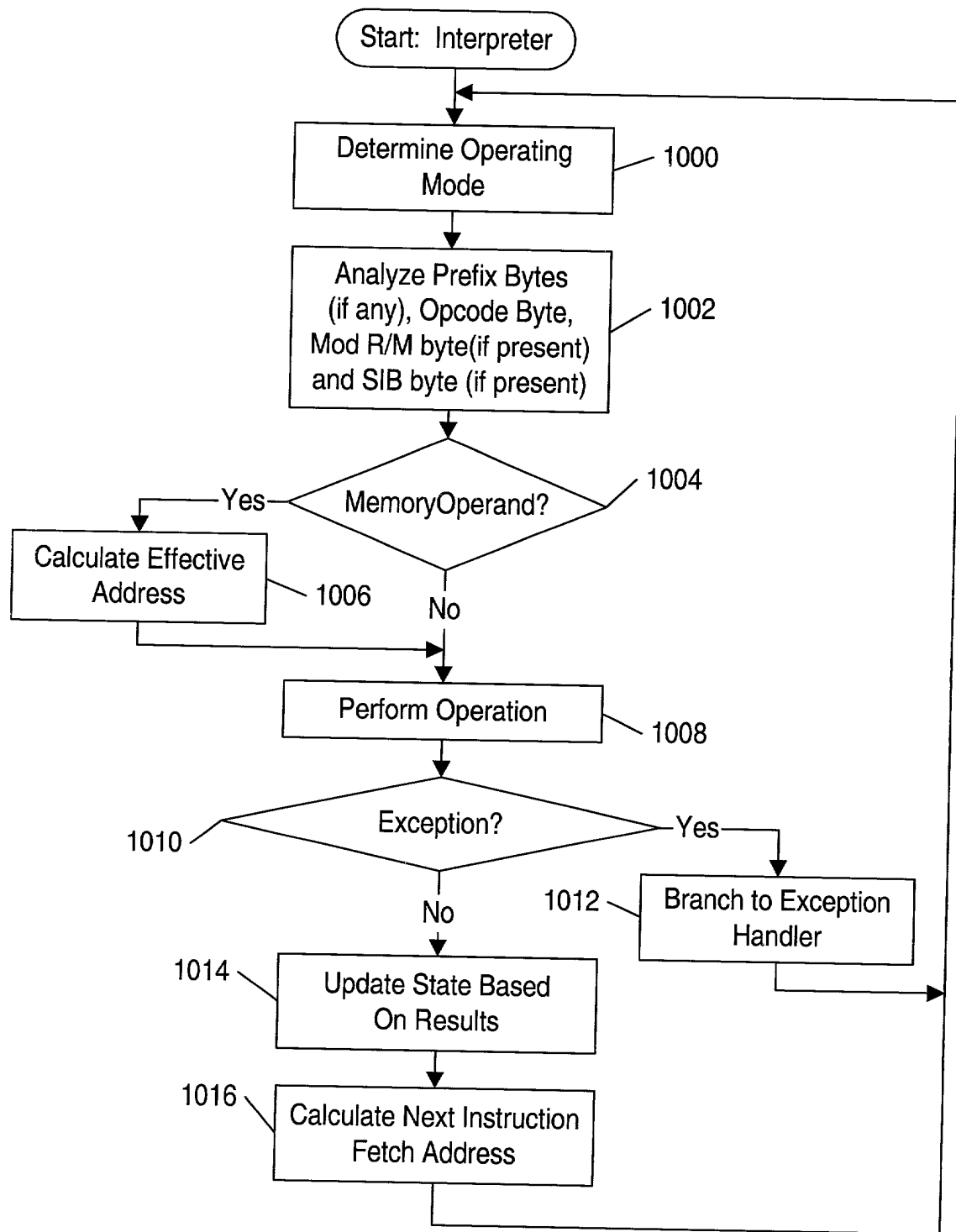
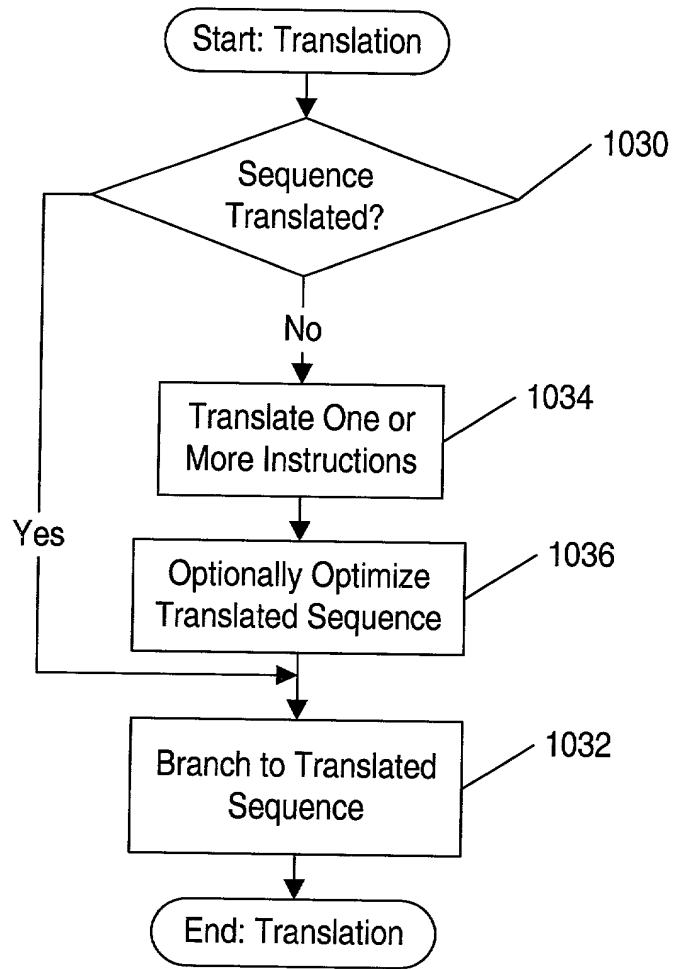


Fig. 7

*Fig. 8*

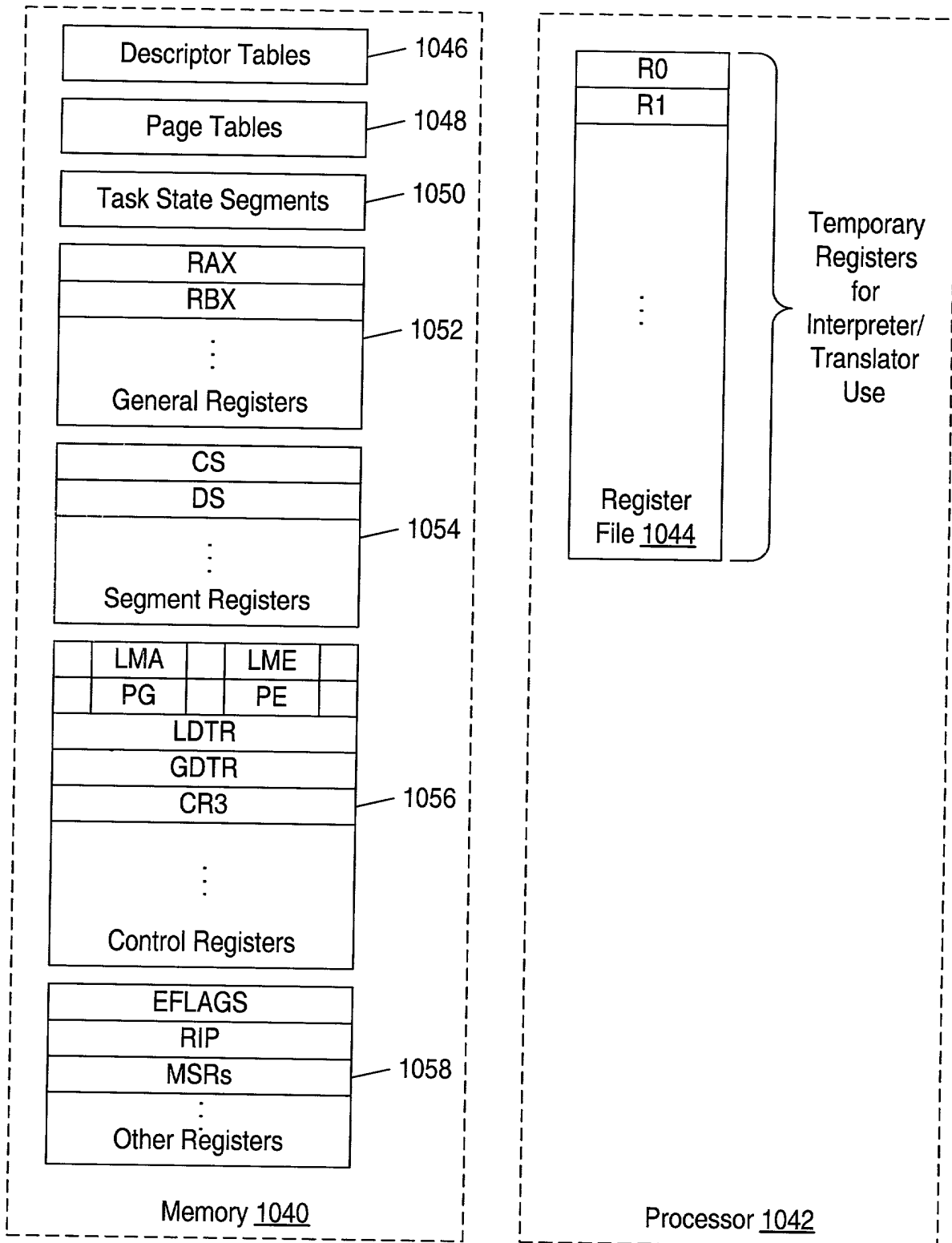


Fig. 9

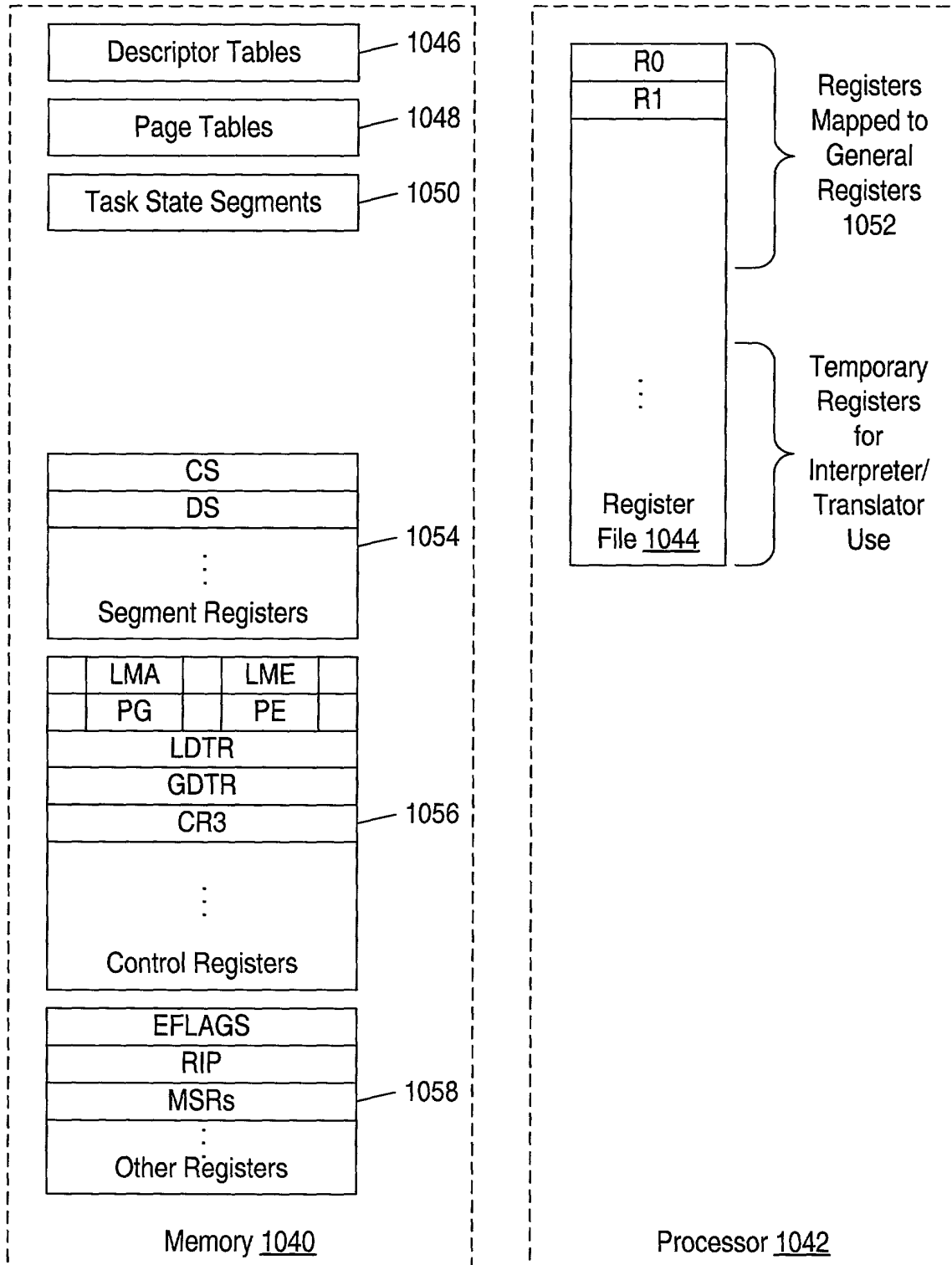


Fig. 10

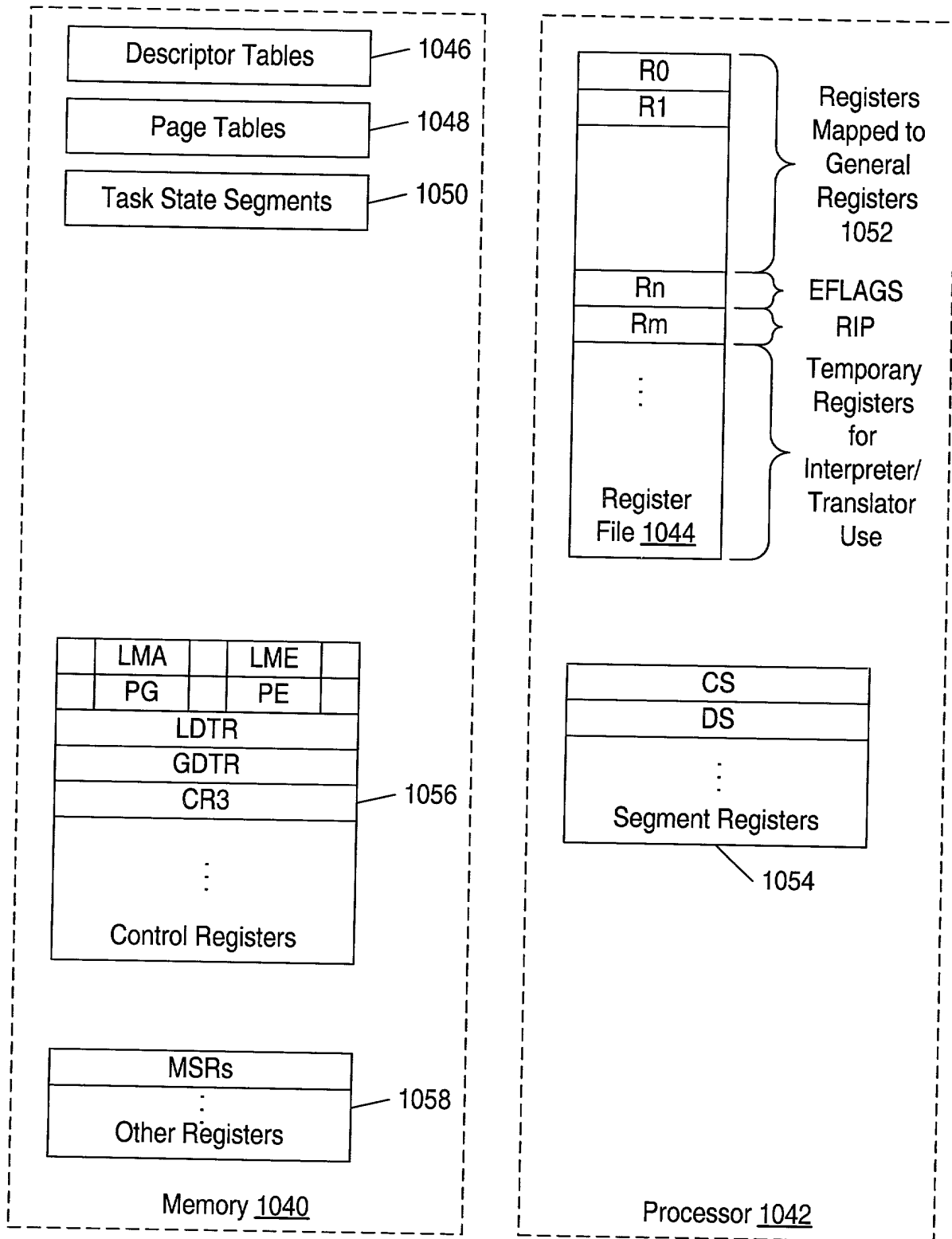


Fig. 11

2

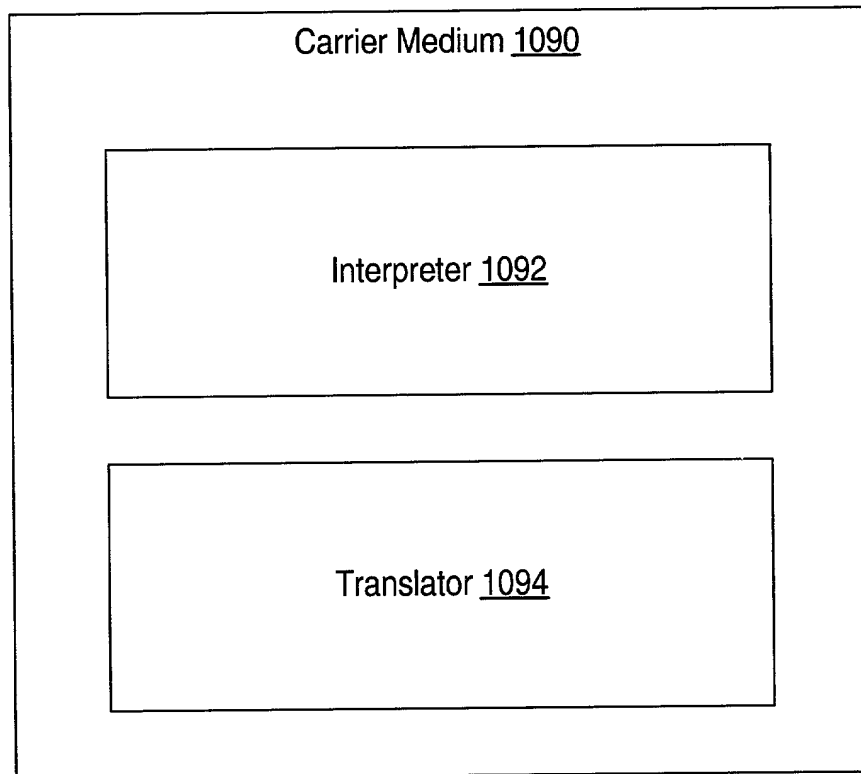


Fig. 12

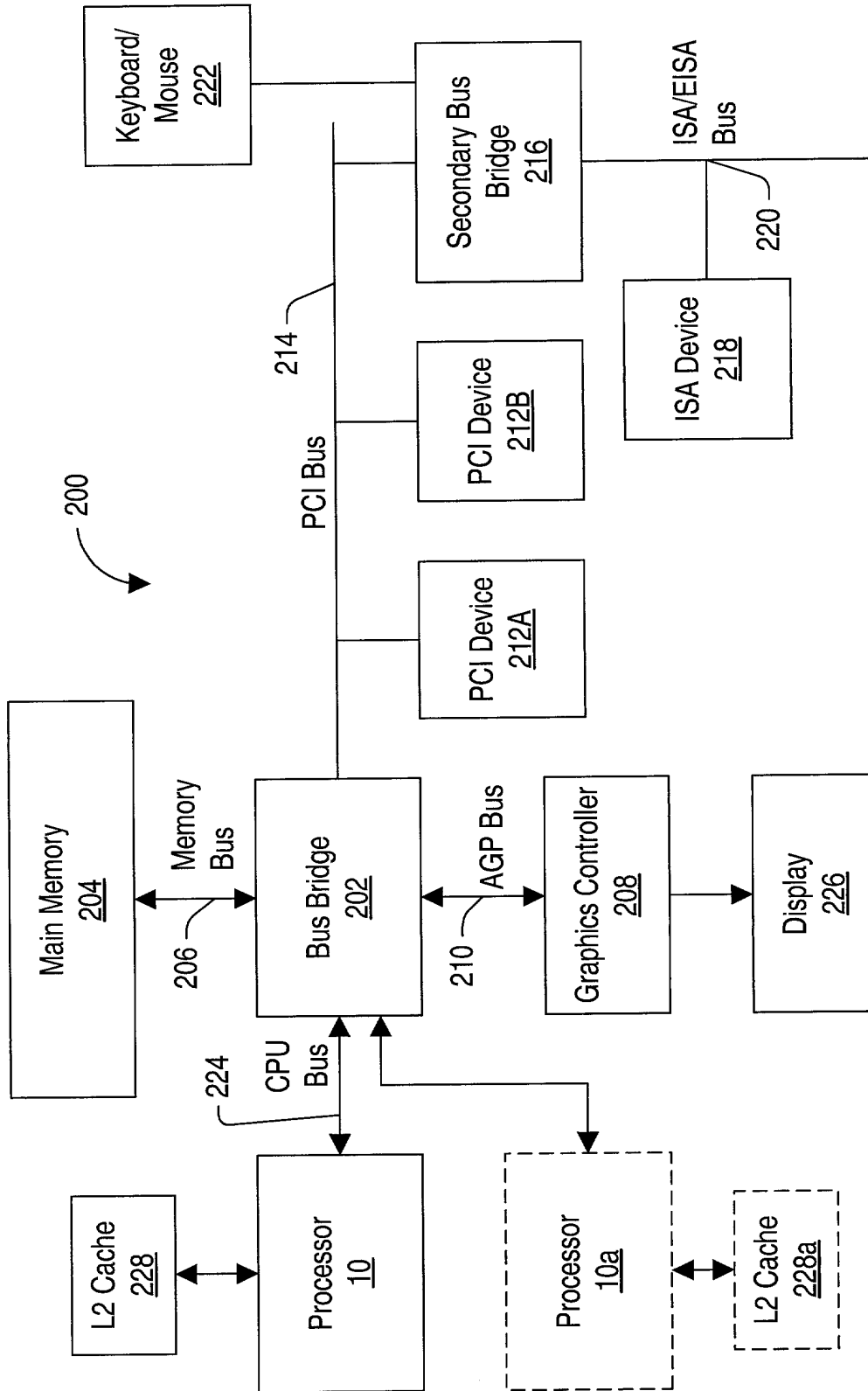


Fig. 13

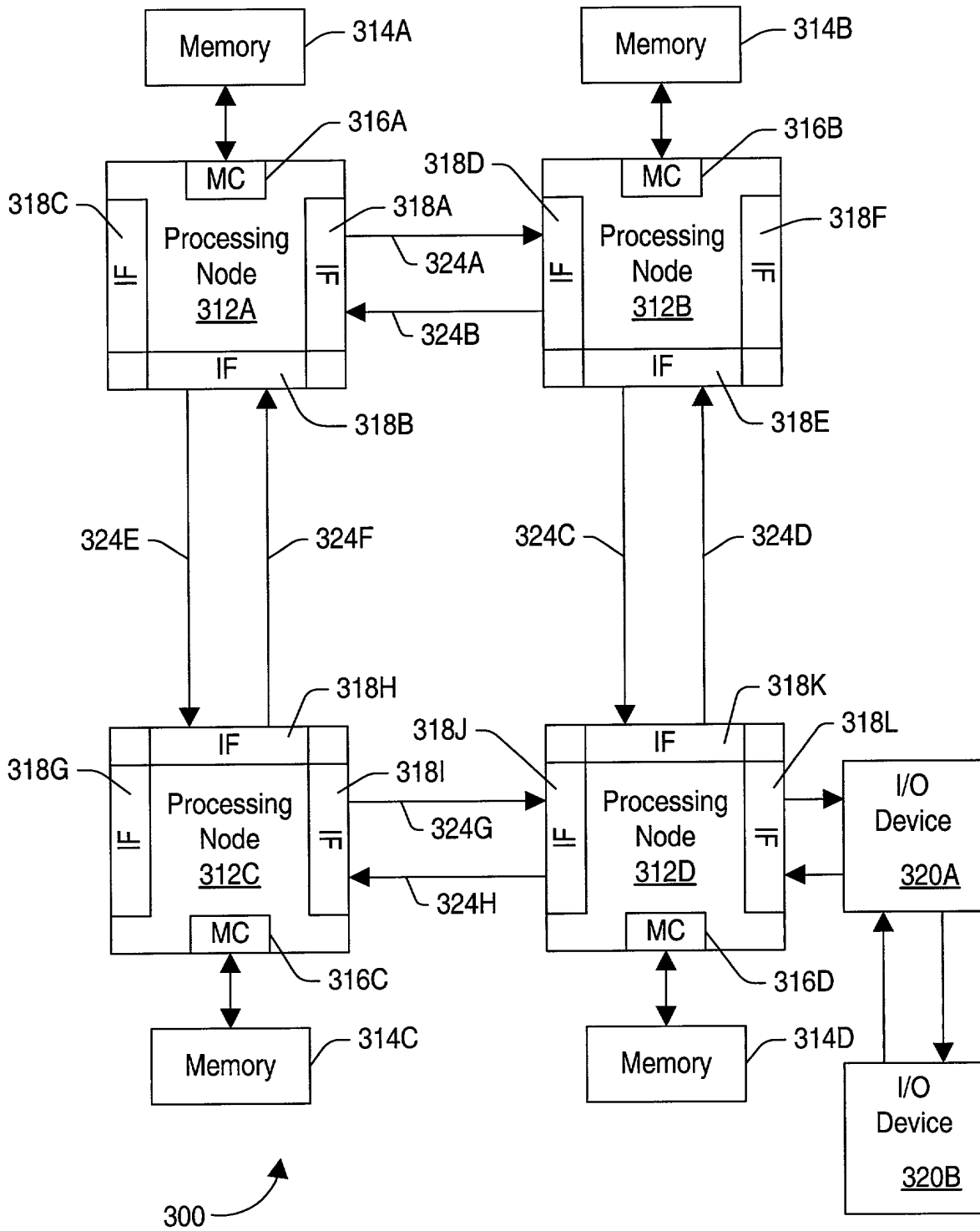


Fig. 14